PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Raymond J. Beffa

Serial No.: 10/791,193

Filed: March 2, 2004

For: SORTING A GROUP OF INTEGRATED CIRCUIT DEVICES FOR THOSE DEVICES REQUIRING SPECIAL TESTING

Confirmation No.: 1963

Examiner: R. Patel

Group Art Unit: 2121

Attorney Docket No.: 2269-3039.4US
(96-0969.04/US)

Notice of Allowance Mailed:

November 22, 2005

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EL995985642US

Date of Deposit with USPS: February 21, 2006

Person making Deposit: Timothy Palfreyman

TRANSMITTAL LETTER

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant submits herewith Part B - Fee(s) Transmittal for the above-captioned application and a Request to Apply Previously Paid Issue Fee to Issue Fee Required by New Notice of Allowance.

Also, enclosed are Comments on Statement of Reasons for Allowance (3 pages); and Fee Addressee for Receipt of PTO Notices Relating to Maintenance Fees (2 pages).

Applicant understands that no additional fees are required. However, if the Office determines that any comparison fees or other additional fees are required, the Commissioner is authorized to charge any such fees to TraskBritt Deposit Account No. 20-1469. A copy of this Transmittal Letter is enclosed for deposit account charging purposes.

Respectfully submitted,

James R. Duzan
Registration No. 28,393
Attorney for Applicant(s)
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: February 21, 2006
JRD/ps:lmh

Enclosures: Part B - Issue Fee Transmittal
Copy of Transmittal Letter
Request to Apply Previously Paid Issue Fee to Issue Fee Required by New Notice of Allowance (3 pages, with attachment)
Comments on Statement of Reasons for Allowance (3 pages)
Fee Addressee for Receipt of PTO Notices Relating to Maintenance Fees (2 pages)

Document in ProLaw

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COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Examiner indicates:

[T]he prior art of the record fails to teach or fairly suggest in combination with the other elements and features of the claimed invention regarding claims 1-18 and 22-28, a sorting process used for a plurality of integrated circuit devices for grouping a first plurality of inspected integrated circuit devices of a type having an

identification code into a group of integrated circuit devices to undergo a first process and for grouping a second plurality of inspected integrated circuit devices to undergo a second process different than the first process, the process and the method comprising: storing data in association with an individual identification code of each of the integrated circuit devices indicating each of the integrated circuit devices undergoes one of the first process and the second process, said data including at least one of fabrication deviation data, probe data, standard test data, special test data, and enhanced reliability testing data in association with the individual identification code of at least some of the integrated circuit devices; reading the individual identification code of each of the integrated circuit devices; accessing the data stored in association with the individual identification code of each of the integrated circuit devices; and grouping the integrated circuit devices in accordance with the accessed data into those of the plurality of integrated circuit devices to undergo the first process and those integrated circuit devices to undergo the second process and regarding claims 19-21, inspection process for integrated circuit devices from semiconductor wafers, the method comprising: causing each of the plurality of integrated circuit devices on each of the semiconductor wafers to store an individual identification code; separating each of the plurality of integrated circuit devices on each of the semiconductor wafers forming one of a plurality of integrated circuit devices; storing data in association with the individual identification code associated with each of the plurality of integrated circuit devices that indicates each of the plurality of integrated circuit devices to undergo one of a first process and a second process, storing the data including storing the individual identification code by programming each of the plurality of integrated circuit devices on each of the semiconductor wafers to permanently store a unique fuse identification; reading the individual identification code associated with each of the separated integrated circuit devices; accessing the data stored in association with the individual identification code that is associated with each of the separated integrated circuit devices; grouping each of the plurality of integrated circuit devices in accordance with the accessed data into those integrated circuit devices to undergo the first process and those integrated circuit devices to undergo the second process; and testing the grouped integrated circuit devices using the first process and the second process.

Applicants concur with the reasons as stated by the Examiner insofar as they comprise a summary, and are exemplary and not limiting. However, the independent claims as allowed include other and different language than that specified by the Examiner, and the allowed dependent claims include other and further features and elements. Accordingly, the scope of the claims must be determined from the literal language of each as a whole, as well as equivalents thereof.

Respectfully submitted,

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